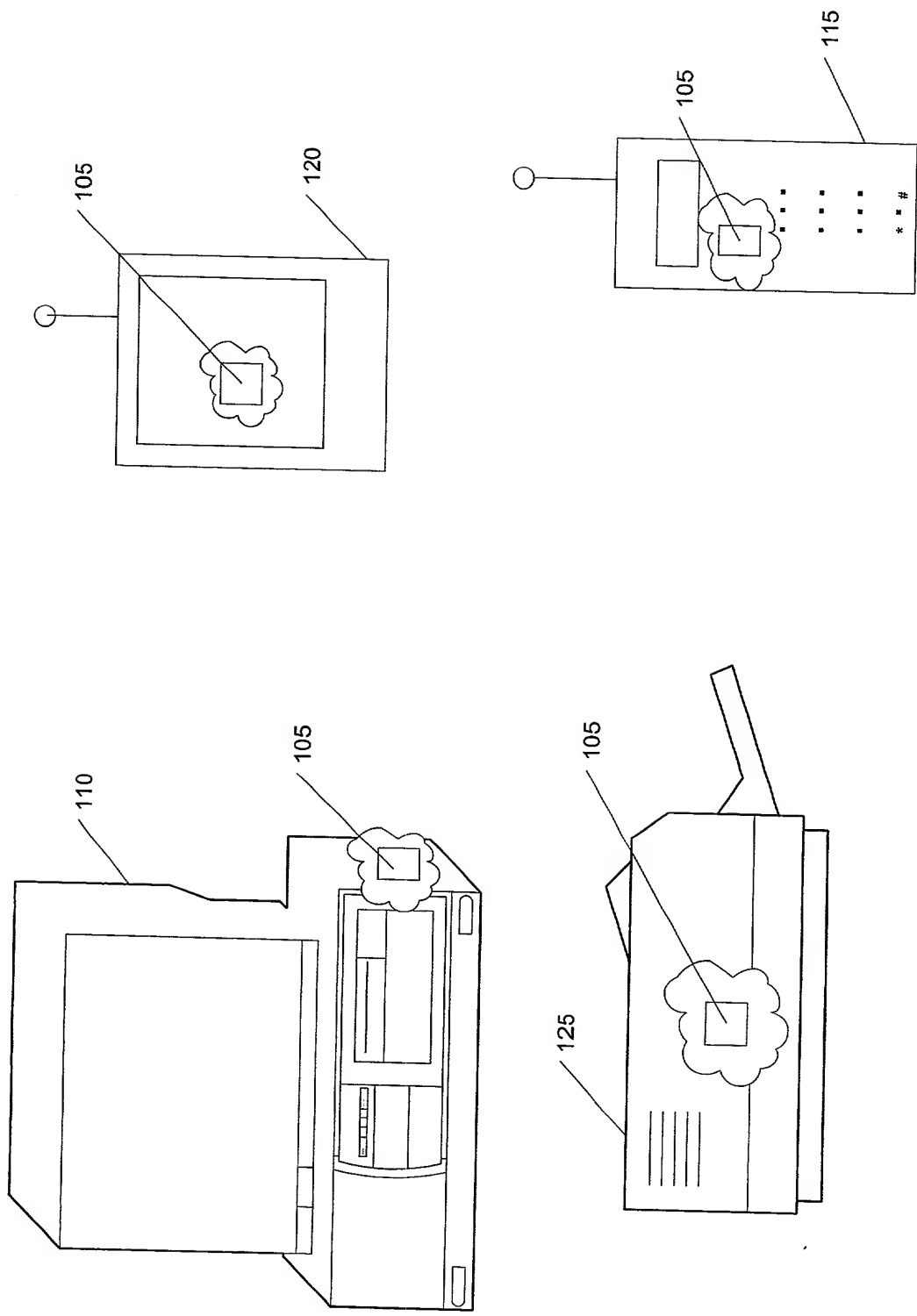
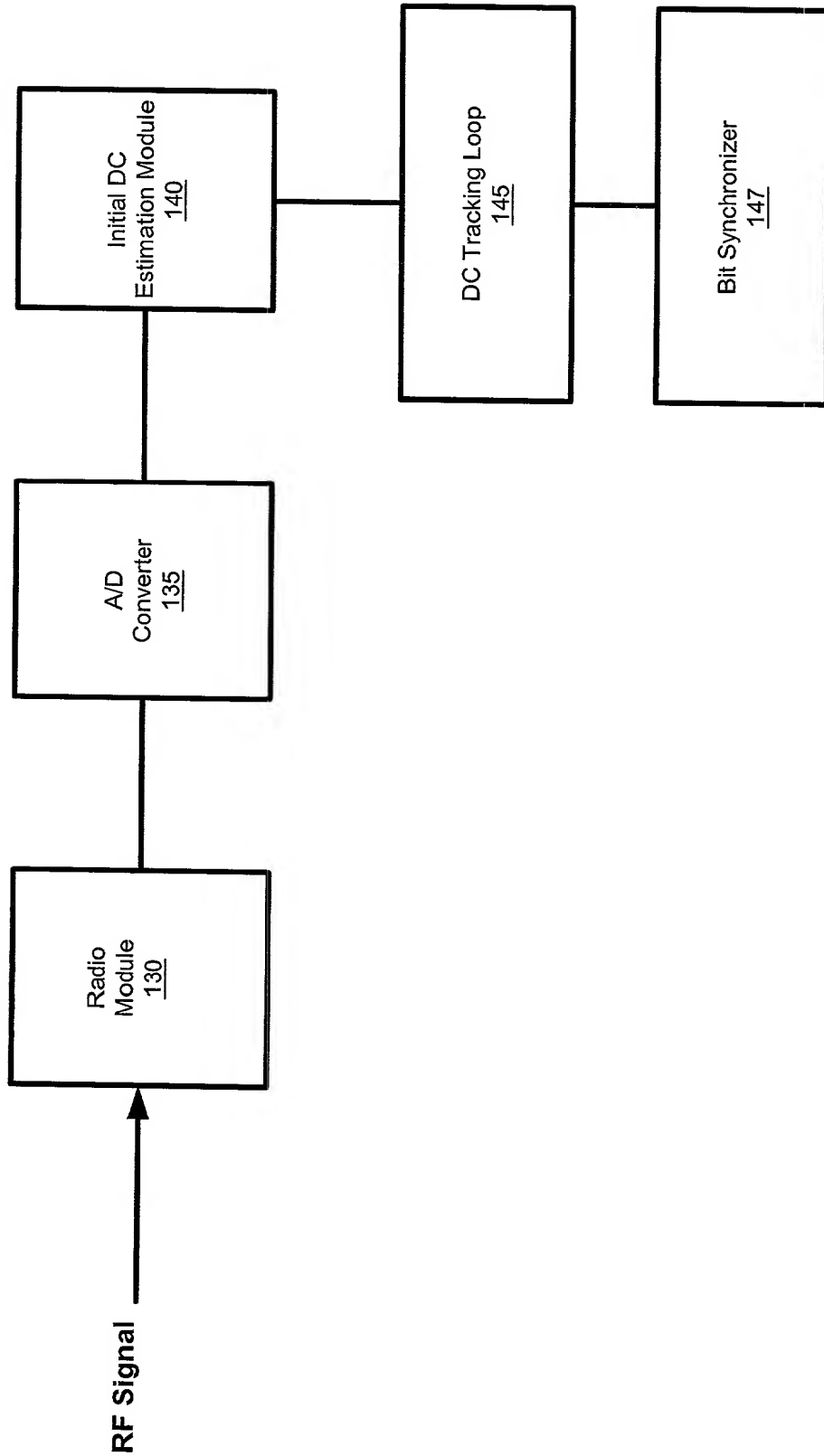


the first and second views of the device are shown in FIG. 1. The first view is a perspective view of the device from the front, and the second view is a perspective view of the device from the side.

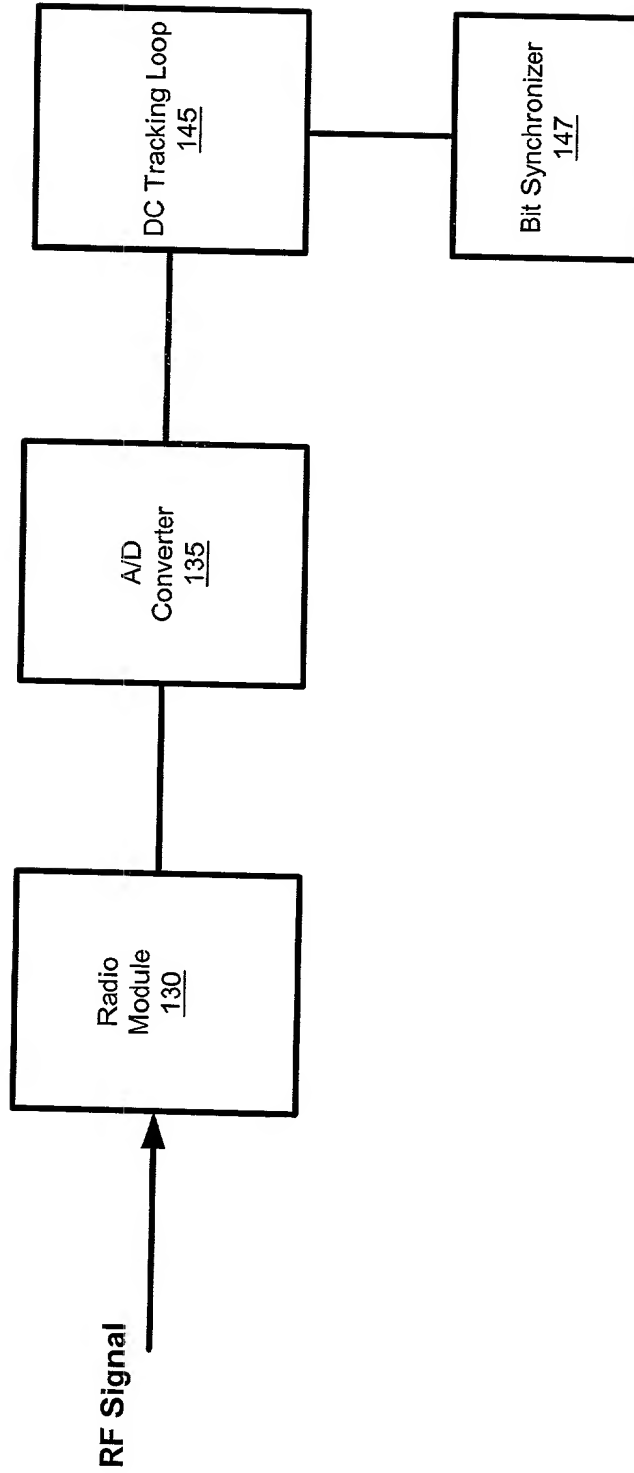


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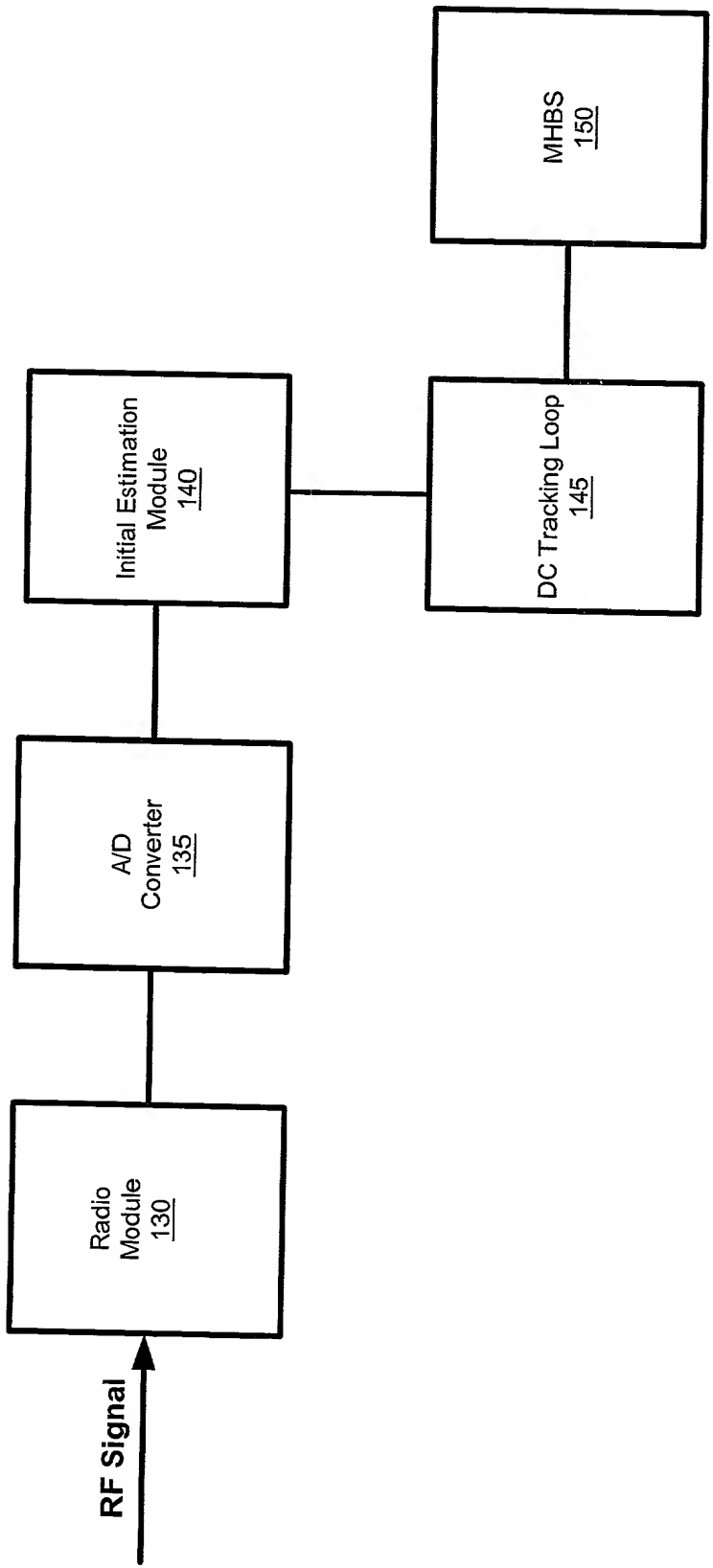
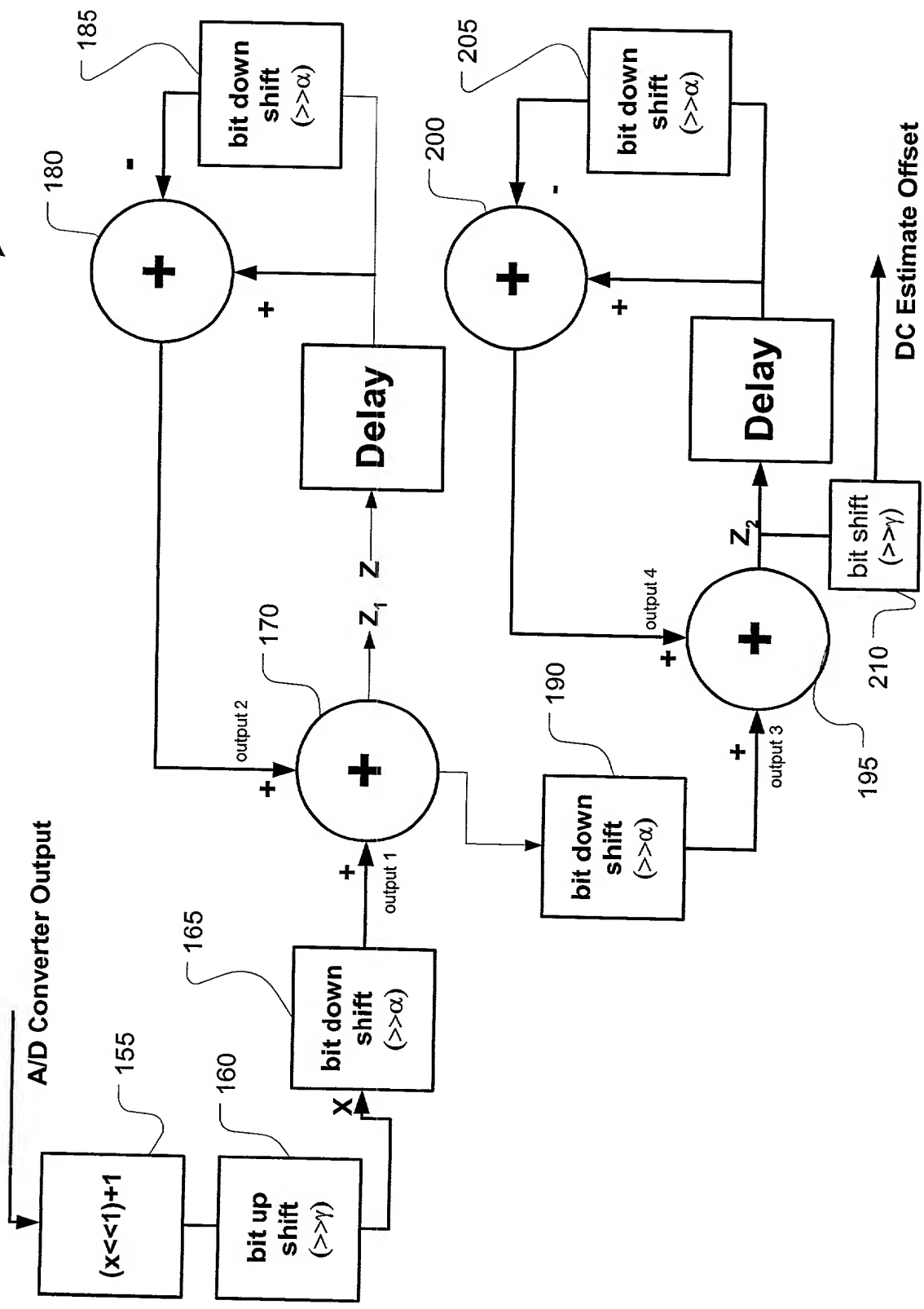


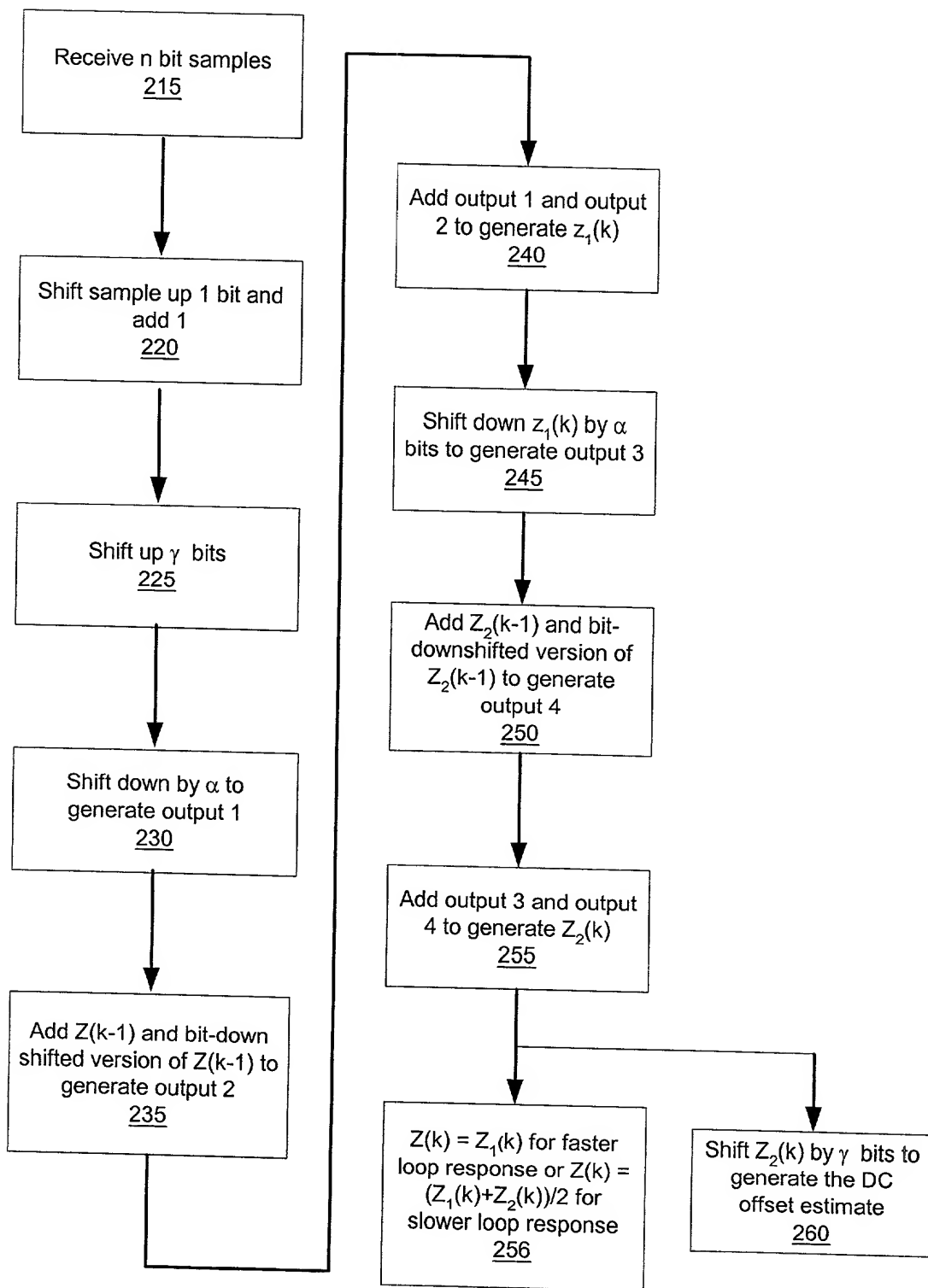
FIG. 5 is a block diagram of a DC estimate offset correction circuit 145. The circuit 145 includes an A/D converter output 155, a bit up shift block 160, a bit down shift block 165, a first adder 170, a delay block 180, a second adder 185, a third adder 190, a delay block 200, a fourth adder 210, and a bit shift block 215. The A/D converter output 155 is input to the bit up shift block 160, which outputs X to the bit down shift block 165. The output of block 165 is input to the first adder 170. The output of the first adder 170 is output 2, which is input to the second adder 185. The output of the second adder 185 is input to the third adder 190. The output of the third adder 190 is output 3, which is input to the fourth adder 210. The output of the fourth adder 210 is output 4, which is input to the second adder 185. The output of the second adder 185 is also input to the delay block 180, which outputs Z₁ to the first adder 170. The output of the third adder 190 is also input to the delay block 200, which outputs Z₂ to the fourth adder 210. The output of the fourth adder 210 is the DC estimate offset.

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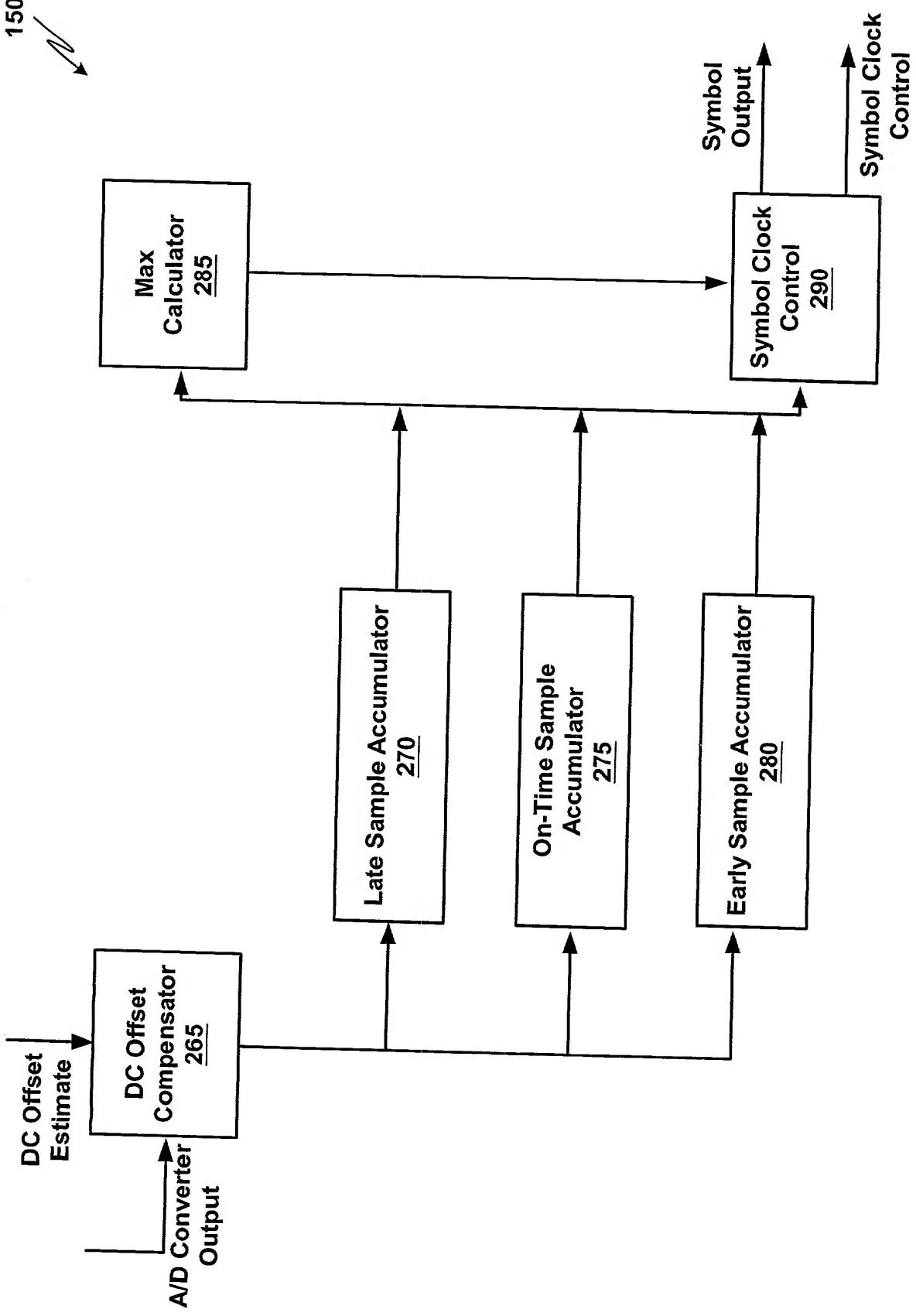
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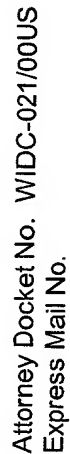
FIGURE 5.



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